

2012 Course: VLIW cores in SoC Architectures

Lecturer: Paolo Faraboschi (Distinguished Technologist, HP Labs)

Total hours:

- Formal Lecture Hours: 18
- Practice Hours: 25-30 (estimated student workload for lab practice and report)
- Tutoring: 3-6 (tools, lab practice Q&A, quiz preparation, report tutoring, evaluation)

Course synopsis

Multicore System-on-Chip (SoC) architectures have been the foundation of high-end embedded system for a decade and have recently appeared in the general purpose computing mainstream in servers and client devices.

This course covers some fundamentals of the SoC market from an industrial perspective and focuses on VLIW cores in the context of high-volume multiprocessor system-on-chip (MPSoC) embedded cores, where VLIW architectures are predominant. The lectures cover all aspects of VLIW processor cores, their architecture and related compilation and evaluation tools.

The goal of the course is to get the students to understand the principles of instruction-level parallelism (ILP), the differences of the various architectural techniques that people have adopted over time (superscalar, pipelining, DSPs, VLIWs), both on architecture and compiler aspects, with a special emphasis on SoC computing. The lectures provide a hands-on, industry-driven perspective on the evolution of the various topics, including a set of “special topics” that cover customization, the role of ILP in power and energy reduction, binary compatibility and a few real example of VLIW-inspired processors.

Detailed syllabus: a bulleted list of subjects; if you like, you can add for each subject the number of hours you give to it, if suitable the tools adopted for practice, etc.)

- Introduction on SoC Computing (2h)
 - Embedded computing landscape, product lifecycle, SoC technologies for low and high volume embedded
 - Evolution of embedded hardware and software, specialization vs. general purpose
 - The role of SoC: how it changes the dynamics and economic, time-to-market, engineering lifecycle, role of VLIW in modern SoCs
- Instruction Level Parallelism and VLIWs (2h)
 - ILP basics, Amdahl's Law and Little Law. Superscalars and VLIW, Limits of ILP
 - Historical notes on compilers, global scheduling, architecture evolution
- VLIW Architectures (4h)
 - VLIW as an architecture, Fetching and issuing wide instructions
 - Register files and clusters

- Branches and the control unit
- Speculation and Predication
- Compiling for VLIW architectures (4h)
 - Engineering of ILP compilers
 - Region formation
 - Trace Scheduling, Superblocks, Loop unrolling, Software pipelining
 - Predication and speculation
 - Schedule construction
- Special Topics (1-2h)
 - Customizable processors
 - Power, energy, VLIWs and DSPs
 - Binary compatibility revisited
- Introduction to the VEX compilation/simulation system (1-2h)
- Real VLIW Architectures (1-2h)

Evaluation: evaluation style adopted (e.g., written exam, project, etc.)

- Quiz (25% weight on final valuation)
 - Closed-book, 2h, covers simple general topics discussed in the lectures
- Lab project using VEX + report on lab project (75% weight on final valuation)
 - One paper per pair of students. Organized as workshop submission, 8 pages, templates provided. Goal of the lab practice is to find the “most efficient” VLIW architecture (performance/\$/Watt/...) and involves: select an application, profile and analyze performance, produce profiling charts, understand where the application spends the time, compute parallelism and resource usage, estimate peak performance for “unlimited resources” vs. a “sequential” machine, tune the application code, add compiler hints, explore different flags, rewrite – if needed – loop kernels to expose more ILP, size the VLIW processor resources and memory parameters, define an architecture space, a “hardware” cost function, an “energy” function; explore the architecture space and find the “best” architecture; investigate usefulness of special operations and find areas of the application that can benefit from ISA customization

References

- J. Fisher, P. Faraboschi, C. Young. “Embedded Computing: A VLIW Approach to Architecture, Compilers and Tools”. Morgan-Kaufmann (Elsevier). ISBN: 1-55860-766-8. Jan 2005. Book website with download links for tools: <http://www.vliw.org>