



Syllabus

ALaRI

Master of Engineering in Embedded Systems Design

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MICROELECTRONICS

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Dates of the course

First Quarter, November 2001, 36hours

Overview of the course

Summary

This course describes microelectronic technologies used to implement integrated circuits. In the design of embedded systems and Systems on Chip (SoC), one would be more and more capable of integrating all the system components on a single chip. It is therefore mandatory to have a good knowledge of what are these microelectronic technologies.

The course contains 4 chapters. The two first chapters describe the design of layout and CMOS circuits in a bottom-up approach. It starts with the first chapter in which layout design is presented while using old but simple technologies to be clearer. The second chapter describes the design of simple CMOS circuits using

simple methods that directly give transistor schematics. Basic cells that can be found today into standard cell libraries will be designed as examples.

The two last chapters are focused on deep submicron technologies as well as on low-power design. The SIA Roadmap will be presented. It describes the possible evolution of microelectronic technologies for the next 15 years and the problems that will occur. The use of such technologies for SoC is mandatory, as these SoC will contain a very large number of transistors. One obvious problem is the power consumption, and the fourth chapter will describe the power consumption issues and the possible solutions at circuit and layout levels.

Outline

Chapter 1: Layout Design
Chapter 2: Design of CMOS Cells
Chapter 3: Microelectronic Technology Evolution
Chapter 4: Low-Power Design at Circuit and Layout Levels

CHAPTER 1. Layout Design

Abstract

This chapter will describe the design of integrated circuits while starting with microelectronic technologies and layout, i.e. the lowest level. Layout rules as well as fabrication process will be introduced, in order to be capable of deriving MOS delay models.

Outline

1.1. Introduction to IC Technologies
1.2. Layout, Masks, Fabrication, Layout Rules
1.3. MOS Transistor, Logical and Delay Models, Logic Gates
1.4. Exercises

Chapter 2. Design of CMOS cells

Abstract

Using N-ch and P-ch MOS transistors, CMOS logic gates will be described. Well-known Karnaugh simplification methods will be reviewed for CMOS design, i.e. static logic, transmission-gate, tri-state and precharged CMOS gates. The latter can be extended to the design of PLAs and ROM memories. Embedded FPGAs, finite state machines, arithmetic units and standard cell libraries will also be presented

Outline

2.1. Introduction
2.2. Combinatorial CMOS Logic
2.3. CMOS Combinatorial Circuits.
2.4. Conduction Functions
2.5. Simple Combinatorial Circuit
2.6. CMOS Gate Synthesis
2.7. Dual Topological Method
2.8. Taxonomy of combinatorial circuits
2.9. Circuits with transmission MOS or Gates
2.10. Tristate gates
2.11. Precharged Combinatorial Logic Circuits
2.12. DOMINO and NORA Logic
2.13. Precharge Logic: Charge Sharing

- 2.14. PLA
- 2.15. ROM Memory
- 2.16. Universal Logic Function
- 2.17. Embedded FPGA (FIPSOC, etc)
- 2.18. Synchronous sequential circuits
- 2.19. Finite State Machines
- 2.20. Arithmetic Basic Cells
- 2.21. Exercises

Chapter 3. VLSI Technology Evolution

Abstract

Deep sub-micron technologies are today used for the design of very powerful microprocessors. The technology progress, from the invention of the transistor (1947) and of the integrated circuits (1958), is spectacular. The evolution from today for the next 15 years can be described while using the 1997 and 1999 up-date SIA Roadmap of the Semiconductor Industry Association. Two main problems can be pointed out, i.e. the power consumption and the interconnect delays. The latter is a problem for the clock synchronization, requiring a careful look at asynchronous architectures. Low-voltage and low-power digital design has also to be applied efficiently to reduce the expected huge power of the future microprocessors. A third problem is the management of the huge complexity of chips with about a Billion transistors. Design methodologies, CAD tools and design reuse have to be revisited to find a efficient way to design such chips.

Outline

- 3.1. Technology Status and Evolution towards Deep Submicron
- 3.2. Interconnect Delays
- 3.3. Design Methodologies, CAD Tools and Intellectual Property (I.P.)

Chapter 4. Low-Power Digital Design

Abstract

Low-voltage and low-power digital design has to be performed at several levels such as system, architecture, logic and layout levels, while considering activity, capacitance, frequency and supply voltage reduction. Comparison of energy-efficient architectures will be performed while using energy/operation and throughput. At the architecture level, power reduction techniques will be presented for reducing activity, V_{dd} without performance degradation and capacitance. Gated clocks finite state machines, asynchronous architectures, pipelining, parallelization and adiabatic techniques are described with some examples. At the circuit and layout level, the power reduction techniques are less efficient than at high level, but some techniques will be presented such as latch-based designs, V_{dd} and V_T reduction, complex gate decomposition and the design of branch-based low power libraries.

Outline

- 4.1. Introduction
- 4.2. Power and Energy, Power Reduction from High to Low Level
- 4.3. Architecture Level: activity reduction, low activity code, gated clocks, asynchronous
- 4.4. Architecture Level: V_{dd} reduction, pipelining, parallelization, adiabatic
- 4.5. Architecture Level: capacitance reduction, simplicity
- 4.6. Low level: latch design, activity reduction, gated clocks, and glitches
- 4.7. Low level: V_{dd} and V_T reduction
- 4.8. Low level: capacitance reduction, low-power library

Notes on the Instructor

Dr. Piguet received his M.S. and Ph. D. degrees in Electrical Engineering from the Ecole Polytechnique Fédérale de Lausanne, respectively in 1974 and 1981.

He joined the Centre Electronique Horloger S.A., Neuchâtel, Switzerland, in 1974. He worked on CMOS digital integrated circuits for the watch industry, low-power embedded microprocessors and CAD tools based on a gate matrix approach. Dr. Piguet is now Head of the Ultra-Low-Power Sector at the CSEM (Centre Suisse d'Electronique et de Microtechnique S.A), Neuchâtel, Switzerland. He is presently involved in design and management of low power and high speed integrated circuits in CMOS technology. His main interests include design of very low-power microprocessors, low-power standard cell libraries, gated clock and low-power techniques as well as asynchronous design.

He is Professor at the Ecole Polytechnique Fédérale Lausanne (EPFL), Switzerland, he also lectures in VLSI and microprocessor design at the University of Neuchâtel, Switzerland, as well as other postgraduate courses in low-power design.