



# Syllabus

**ALaRI**

**Master of Engineering in Embedded Systems Design**

**University of Lugano**

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## ARCHITECTURES

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### Dates of the course

First Quarter, October 2001, 36 hours

### Overview of the course

The course deals with advanced computer architectures, giving particular attention to aspects of interest for embedded systems. Topics include, but are not limited to, cache architecture and organization, pipelined

CPUs, Instruction-Level Parallelism in CPUs (with particular reference to superscalar architectures), DSP CPUs, and multiprocessor architectures.

Suggested textbook: J. Hennessey, D. Patterson "Computer Architecture: a quantitative approach" 3<sup>d</sup> edition, Morgan-Kaufmann Publishers.

The course includes lectures, exercises and practice. Evaluation is based on class projects that are assigned to individual students or small groups of students.

*Architectures*: Basic definitions. The bottlenecks in the Von Neumann paradigm

*Cache memories*: principles. Alternative organizations; figures of merit, performance evaluation. Cache management issues. Multiple-level caches.

*Innovative CPU architectures*: basic figures of merit for performance evaluation. Pipelining: the RISC approach – hints at pipelined CISC CPUs. The basic MIPS pipeline. Hazards: resource hazards, data hazards, control hazards. Overcoming hazards in the basic pipeline. Exception handling.

*ILP architectures*: the basic idea. Dynamic scheduling, static scheduling. Superscalar architectures: basic principles and problems. Out-of-order execution and its management. Scoreboarding, reservation stations, the Reorder Buffer. Hazard problems and management in superscalar CPUs. Speculative execution and its optimization. Exception handling. Reference to some real-world superscalar CPUs. Basic characteristics of DSP processors

*Multiprocessor systems*: basic solutions. Shared-memory systems, message-passing systems. Caches in multiprocessor systems. The cache coherence problem. NUMA, CC-NUMA systems. Basic concepts of multithreading: simultaneous multithreading, speculative multithreading.

## Notes on the Instructor

Mariagiovanna Sami is Professor, Digital Processing systems, at Politecnico di Milano. She holds an Electronics Engineer degree (Politecnico di Milano, 1966) and a Libera Docenza, Switching Theory and Computing (Italian Ministry for Education, 1971).

Her research interests include various aspects of digital architecture design, with particular reference to defect and fault-tolerance of digital architectures, parallel architectures, low-power design and high-level synthesis. She is co-author and/or co-editor of several books and of over 200 technical papers. She has been Chairman of the Department of Electronics, Politecnico di Milano, and is at present Scientific Director of the ALaRI Institute, University of Lugano.

Pro. Sami has been Editor-in-Chief of the Journal of Systems Architecture and member of the Board of Editors of IEEE Micro, IEEE Design and Test, IEEE Transactions of computers. She is a member of the Board of Editors of JETTA - Journal of Electronic Testing. She was General Chair or Program Chair for a number of international conferences chair; in 2000 she was General chair of IJCNN (the International Joint Conference on Computer Networks). She was also co-director of the NATO Advanced Study Institutes on VLSI Testing held in Como, Italy, in 1985 and on Hardware/Software co-design held in Tremezzo (Italy) in 1995.